WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

functional circuitry, coupled to a terminal; and

an electrostatic discharge protection device connected to the terminal in parallel with the functional circuitry, and formed at a semiconducting surface of a substrate, comprising:

a first well of a first conductivity type, disposed at the surface within a portion of the substrate of the second conductivity type;

a first doped region of a first conductivity type, disposed within the first well;

a second doped region, of a second conductivity type, disposed within the first well and connected to the terminal; and

a grounded doped region, disposed at the surface within a portion of the substrate of the second conductivity type;

wherein a compensated well portion of the first well underlying the second doped region has a lower net number of impurities than other portions of the first well.

2. The integrated circuit of claim 1, further comprising:

a second well, of the second conductivity type, disposed at the surface;

wherein the grounded doped region is disposed within the second well.

3. The integrated circuit of claim 2, wherein the second well overlaps with the first well at a location underlying the second doped region, to form the compensated well portion of the first well.

4. The integrated circuit of claim 1, further comprising:

a third doped region, of the second conductivity type and disposed within the first well, the third doped region connected to the grounded doped region; and

a transistor gate insulatively disposed between the second and third doped regions, and connected to the terminal.

5. The integrated circuit of claim 1, wherein the first and second doped regions are separated from one another at the surface of the first well by an isolation oxide structure.

6. The integrated circuit of claim 5, wherein the isolation oxide structure is disposed within a trench formed at the surface.

7. The integrated circuit of claim 1, wherein the first conductivity type is n-type and the second conductivity type is p-type.

8. The integrated circuit of claim 1, wherein each of the first and second doped regions, and the grounded doped region, are clad with a metal silicide.

9. The integrated circuit of claim 1, further comprising:

a second well, of the second conductivity type, disposed at the surface, within which the grounded doped region is disposed;

wherein the second well overlaps with the first well at a location underlying the second doped region, to form the compensated well portion of the first well;

and wherein the grounded doped region is of the first conductivity type.

10. The integrated circuit of claim 9, further comprising:

an overlapping doped region of the first conductivity type, formed at the surface at a boundary location between the first and second wells, the overlapping doped region coupled to the terminal.

11. The integrated circuit of claim 10, wherein the grounded doped region and the overlapping doped region are separated from one another at the surface by an isolation oxide structure.

12. The integrated circuit of claim 11, wherein the isolation oxide structure is disposed in a trench at the surface.

13. The integrated circuit of claim 10, wherein the grounded doped region and the overlapping doped region are separated from one another at the surface of the second well;

and further comprising:

a gate electrode insulatively disposed over the portion of the surface of the second well separating the grounded doped region and the overlapping doped region, and coupled to the grounded doped region.

14. The integrated circuit of claim 9, further comprising an isolation oxide structure disposed adjacent to the second doped region;

and further comprising:

a gate electrode insulatively disposed over a portion of the first and second wells, adjacent to the grounded doped region, and extending onto the isolation oxide structure, the gate electrode coupled to the grounded doped region.

15. The integrated circuit of claim 9, further comprising:

an overlapping doped region formed at the surface at a boundary location between the first and second wells;

a first gate electrode, coupled to the terminal, and insulatively disposed over a portion of the first well between the second doped region and the overlapping doped region;

a second gate electrode, coupled to the grounded doped region and insulatively disposed over a portion of the second well between the overlapping doped region and the grounded doped region; and

an isolation oxide structure disposed between the first and second doped regions at a surface of the first well.

16. The integrated circuit of claim 15, wherein the overlapping doped region is of the first conductivity type.

17. The integrated circuit of claim 15, wherein the overlapping doped region is of the second conductivity type.

18. The integrated circuit of claim 15, wherein the overlapping doped region comprises a doped region of the first conductivity type adjacent to a doped region of the second conductivity type.

19. The integrated circuit of claim 1, wherein the first doped region is connected to the terminal.

20. The integrated circuit of claim 1, wherein the first doped region is connected to a power supply bus of the integrated circuit.

21. The integrated circuit of claim 1, further comprising:

an overlapping doped region of the first conductivity type, formed at the surface at a boundary location of the first well;

a first silicide block structure disposed between the overlapping doped region and the second doped region;

a second silicide block structure disposed between the overlapping doped region and the grounded doped region;

a source region, of the first conductivity type, formed at the surface outside of the first well; and

a gate structure, disposed between the first doped region and the source region, and overlying a boundary location of the first well, to define a drain-extended transistor;

wherein each of the first and second doped regions, the overlapping doped region, and the grounded doped region, are clad with a metal silicide.

22. A method of fabricating an ESD protection device for an integrated circuit, comprising:

forming isolation oxide structures at selected locations of a semiconducting surface of a substrate;

ion implanting dopant corresponding to a first conductivity type at selected locations of the surface to form wells of the first conductivity type;

ion implanting dopant corresponding to a second conductivity type at selected locations of the surface to form wells of the second conductivity type;

wherein a selected location of the surface is implanted with dopant of both the first conductivity type and the second conductivity type, to form a compensated well portion of a first well of the first conductivity type having a lower net number of impurities than other wells of the first conductivity type;

the method further comprising the steps of:

forming doped regions of the first conductivity type at the surface, the doped regions including a first doped region within the first well of the first conductivity type; and

forming doped regions of the second conductivity type at the surface, the doped regions including a second doped region within the first well of the first conductivity type, and overlying at least a portion of the compensated well location,

wherein one of the steps of forming doped regions forms a ground doped region within a portion of the surface of the second conductivity type, near the well of the first conductivity type;

the method further comprising the step of:

forming overlying conductors to connect the second doped region to a terminal, and to connect the ground doped region to a device ground region.

23. The method of claim 22, wherein the step of forming doped regions of the second conductivity type forms a third doped region of the second conductivity type within the well of the first conductivity type;

and further comprising:

forming a gate electrode insulatively disposed over a portion of the well of the first conductivity type between the second and third doped regions.

24. The method of claim 22, wherein the step of forming isolation oxide structures comprises:

forming trenches into the surface of the substrate at selected locations;

depositing an oxide over the surface and into the trenches; and

then planarizing the oxide in the trenches.

25. The method of claim 22, further comprising:

cladding the surface of the doped regions with a metal silicide.

26. The method of claim 22, wherein the step of ion implanting dopant corresponding to the first conductivity type is performed prior to the step of ion implanting dopant corresponding to the second conductivity type.

27. The method of claim 26, wherein one implanted location in the step of forming doped regions of the second conductivity type overlaps an implanted location in the step of forming doped regions of the first conductivity type, to form the compensated well location.

28. The method of claim 22, wherein the step of ion implanting dopant corresponding to the first conductivity type is performed after to the step of ion implanting dopant corresponding to the second conductivity type.

29. The method of claim 28, wherein one implanted location in the step of forming doped regions of the first conductivity type overlaps an implanted location in the step of forming doped regions of the second conductivity type, to form the compensated well location.

30. The method of claim 22, wherein the step of forming doped regions of the first conductivity type also forms an overlapping doped region of the first conductivity type at a boundary of the first well;

and wherein the step of forming overlying conductors also forms a conductor coupling the overlapping doped region to the terminal.

31. The method of claim 30, further comprising:

forming a gate electrode insulatively disposed at a location of the surface between the overlapping doped region and the ground doped region;

and wherein the step of forming overlying conductors also forms a conductor coupling the gate electrode to the ground doped region.

32. The method of claim 22, further comprising:

forming a gate electrode insulatively disposed at a location of the surface between the second doped region and the ground doped region, the gate electrode also overlapping onto an isolation oxide structure disposed at the surface between the second doped region and the ground doped region;

and wherein the step of forming overlying conductors also forms a conductor coupling the gate electrode to the ground doped region.

33. The method of claim 22, wherein one of the steps of forming doped regions also forms an overlapping doped region at a boundary of the first well;

further comprising:

forming gate electrodes at the surface, a first gate electrode insulatively disposed at a location between the overlapping doped region and the second doped region, and a second gate electrode disposed at a location between the overlapping doped region and the ground doped region;

and wherein the step of forming overlying conductors also forms a conductor coupling the first gate electrode to the terminal, and a conductor coupling the second gate electrode to the ground doped region.

34. The method of claim 33, wherein the step of forming the doped regions is performed after the step of forming gate electrodes, so that the doped regions are formed in a self-aligned manner relative to the gate electrodes.

35. The method of claim 3, wherein the overlapping doped region is formed by the step of forming doped regions of the first conductivity type.

36. The method of claim 33, wherein the overlapping doped region is formed by the step of forming doped regions of the second conductivity type.

37. The method of claim 33, wherein a portion of the overlapping doped region is formed by the step of forming doped regions of the first conductivity type, and an adjacent portion of the overlapping doped region is formed by the step of forming doped regions of the second conductivity type.

38. The method of claim 22, wherein the step of ion implanting dopant corresponding to a first conductivity type forms wells of the first conductivity type having a retrograde doping profile.

39. The method of claim 38, wherein the step of ion implanting dopant corresponding to a second conductivity type forms wells of the second conductivity type having a retrograde doping profile.

40. The method of claim 22, wherein the step of ion implanting dopant corresponding to a second conductivity type forms wells of the second conductivity type having a retrograde doping profile.

41. The method of claim 22, wherein the step of forming doped regions of the first conductivity type also forms an overlapping doped region of the first conductivity type at a boundary of the first well, and forms the grounded doped region, of the first conductivity type, outside of the first well;

and further comprising:

forming a first silicide block insulator structure disposed at the surface between the location of the second doped region and the overlapping doped region, and a second block insulator structure disposed at the surface between the location of the overlapping doped region and the grounded doped region; and

cladding the surface of the doped regions with a metal silicide.

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